

Arquitectura VHDL para practicar el algoritmo de simulación

```
architecture prueba2 of ejemplo is
    signal a, b, e, d: bit;
begin
    P: process (a,d) is
        begin
            e <= not d after 2 ns;
            wait for 5 ns;
            b <= not a after 2 ns;
        end process;
    Q: process is
        begin
            b <= b or e after 1 ns;
            d <= (e and d) or a after 3 ns;
            a <= e or (d and b) after 3 ns;
            wait on b,e,d,a;
        end process;
end prueba2;
```