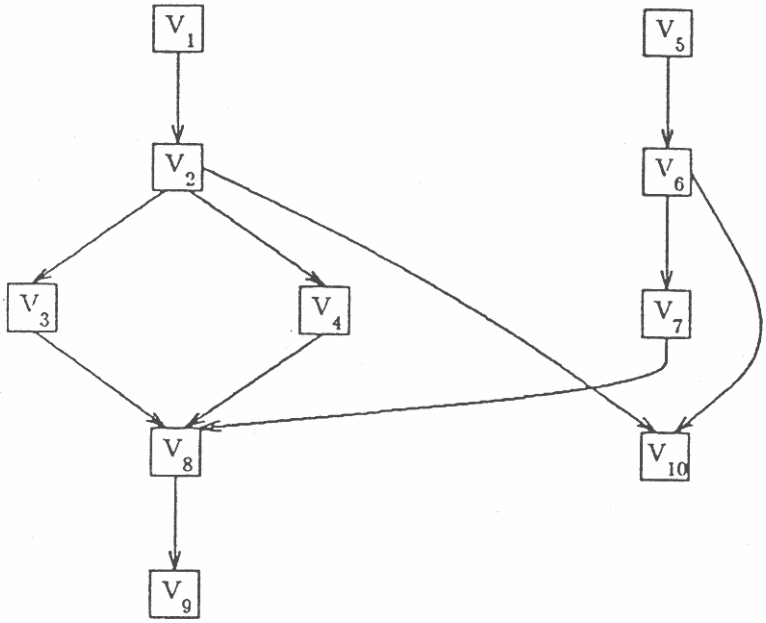
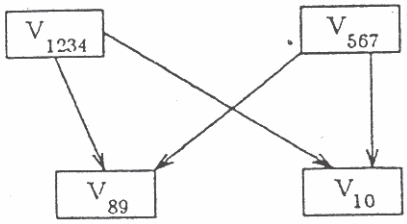
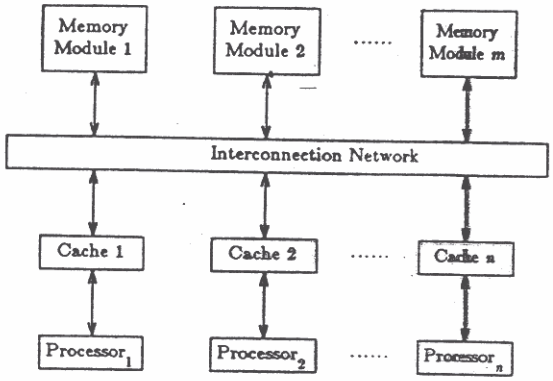


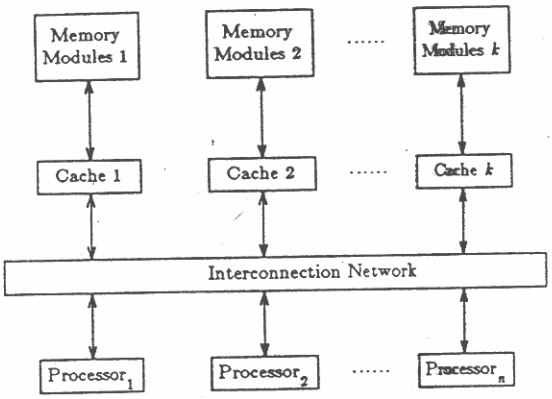
A DDG with instructions as vertices.



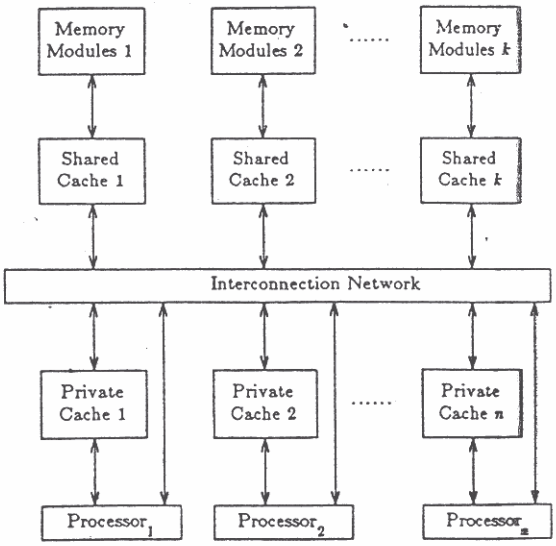
A DDG with instruction groups as vertices.



Multiprocessor with private caches.



Multiprocessor with shared caches.



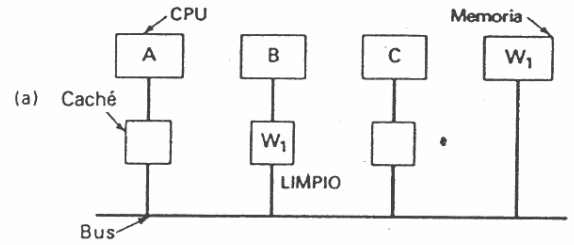
Multiprocessor with combined private and shared caches.

1. INVALIDO —Este módulo de la caché no contiene datos válidos

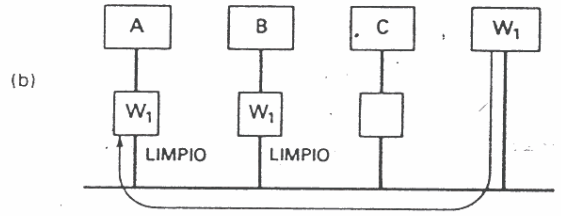
2. LIMPIO —La memoria está actualizada; el bloque puede estar en otras cachés

3. RESERVADO —La memoria está actualizada; ninguna otra caché contiene este bloque

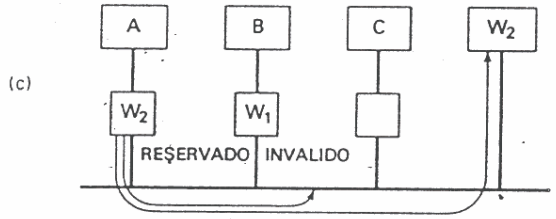
4. SUCIO —La memoria es incorrecta; ninguna otra caché contiene este bloque



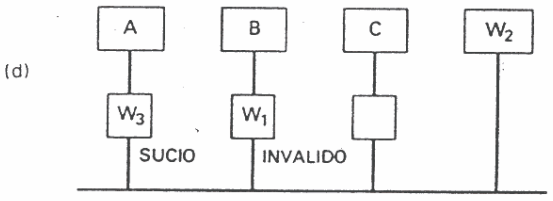
Estado inicial.
W1 está en memoria y en la caché de B.



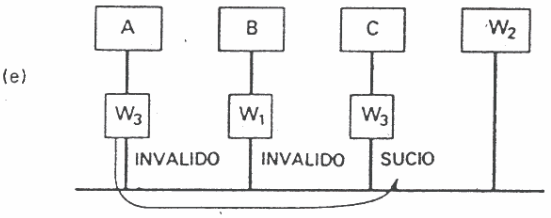
A lee W.
B no reacciona a la lectura de A. El valor viene de la memoria.



A escribe W.
La escritura inicial en la caché de A invalida la copia en la caché de B, actualiza la memoria y marca la copia en A como RESERVADA

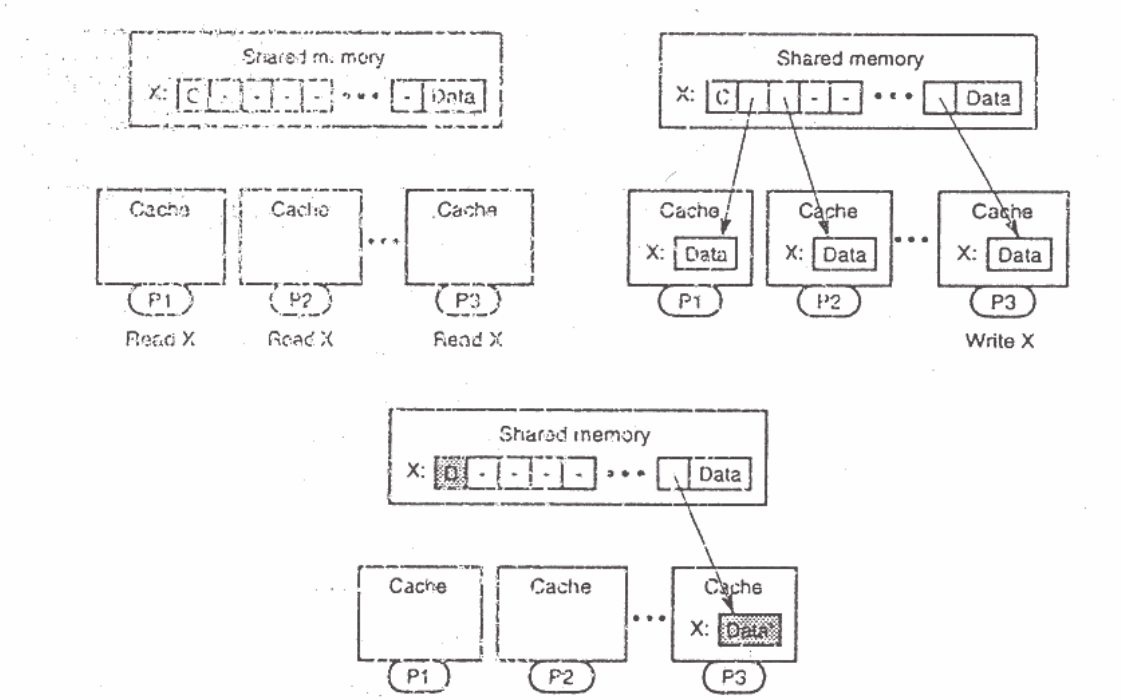


A escribe de nuevo W.
Las escrituras posteriores se realizan en forma local en la caché de A. No se requiere tráfico del bus.

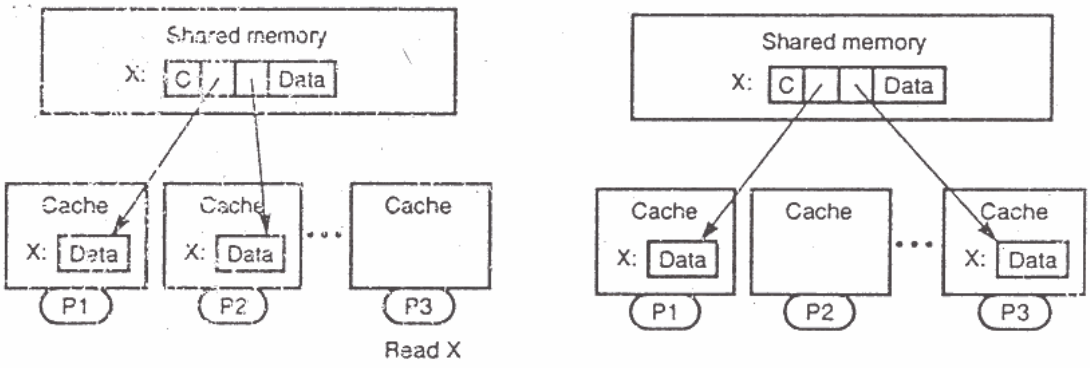


C lee W.
Cuando esto sucede, A proporciona el bloque e invalida el elemento en su caché. Ahora C tiene el único dato válido.

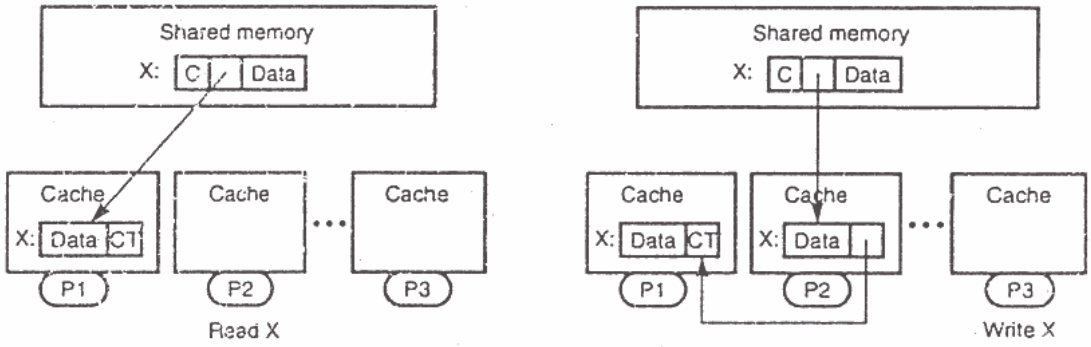
Protocolo de coherencia de la caché *de una sola escritura.*



(a) Three states of a full-map directory

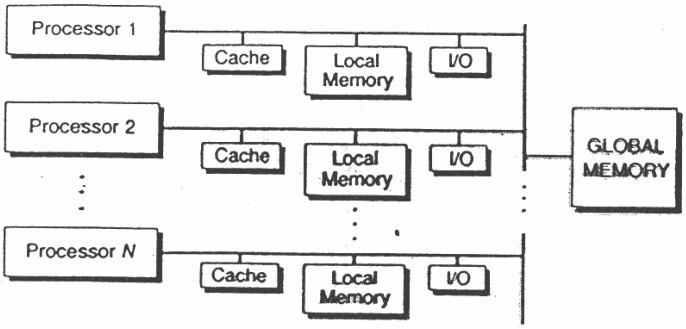


(b) Eviction in a limited directory

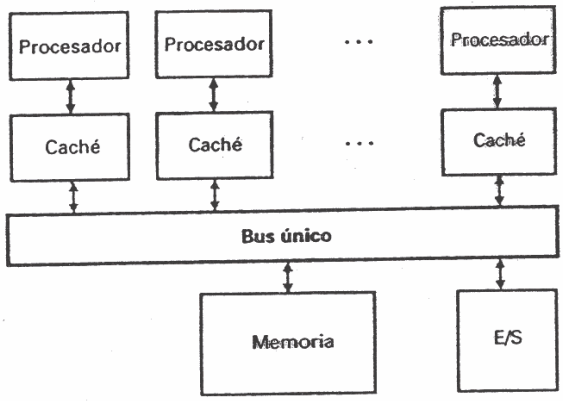


(c) The chained directory

Three types of cache directory protocols.



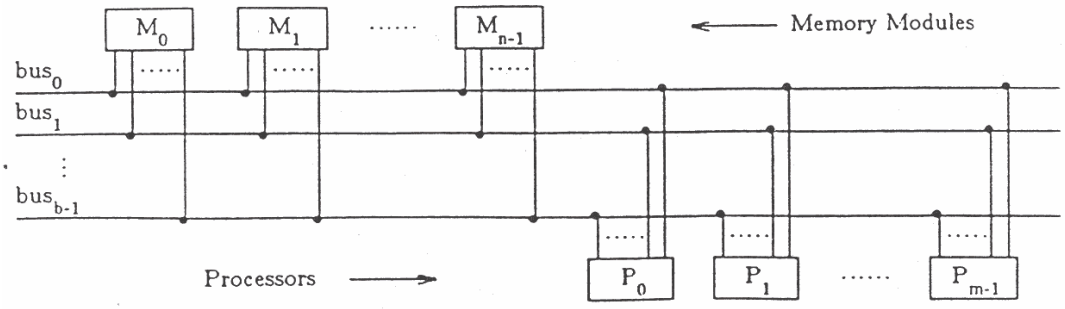
A bus-connected multiprocessor.



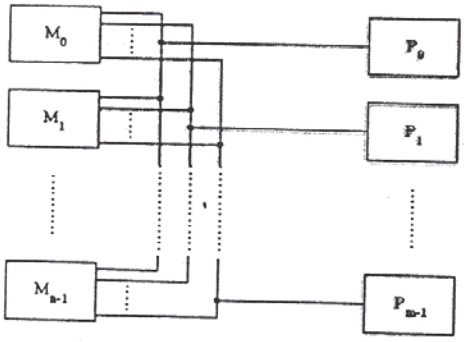
Un multiprocesador de un solo bus. El tamaño típico está entre 2 y 32 procesadores.

Institución	Nombre	Máximo número de proc.	Bits/ proc.	Proc. frec. reloj	Número de FPU	Tamaño máximo memoria/ sistema (MB)	Ancho de banda comunicaciones/ sistema (MB/seg)	Año
Sequent	Symmetry	30	32	16 MHz	30	240	53	1988
Silicon Graphics	4/360	16	32	40 MHz	16	512	320	1990
Sun	4/640	4	32	40 MHz	4	768	320	1991

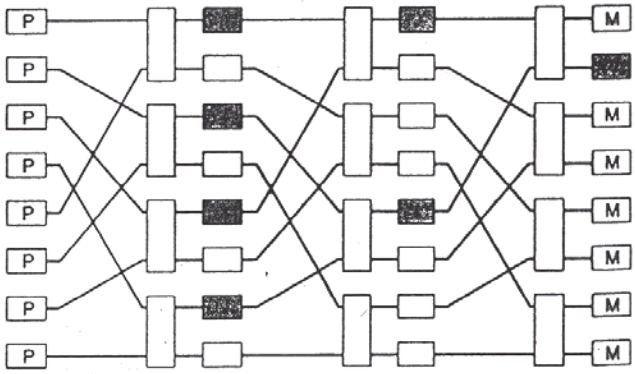
Características de cuatro computadores MIMD conectados por un solo bus de plano posterior. Número de FPU significa número de unidades de punto flotante. La anchura de banda de comunicaciones para estas máquinas es la anchura de banda del bus.



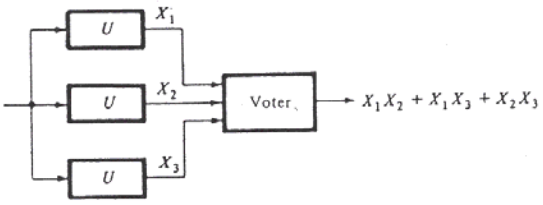
A multiple-bus multiprocessor structure.



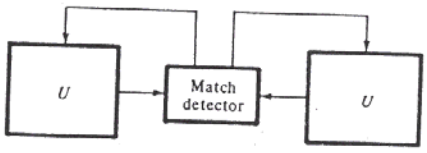
Multiport memories.



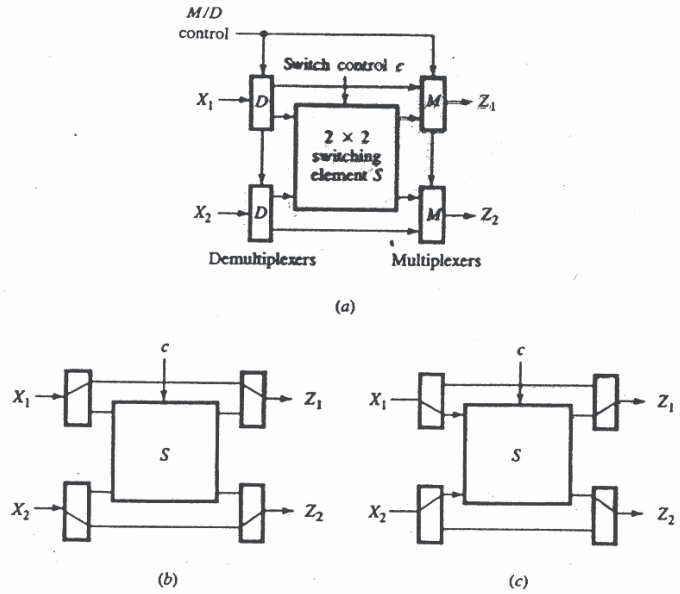
A "hot" spot in a memory module (indicated by shading) and the switching modules that block as a result. The path from Processor 0 (the top processor) to Memory 3 is blocked, although neither Processor 0 nor Memory 3 is very active.



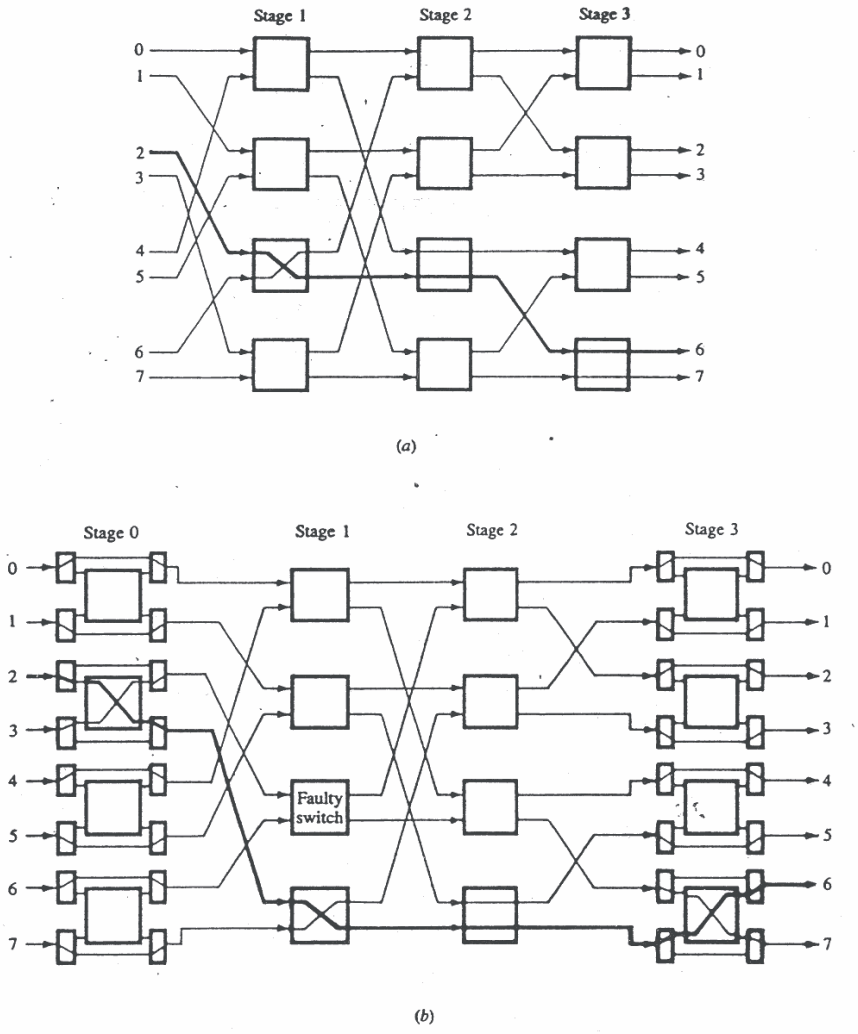
Example of triple modular redundancy (TMR).



Fault-tolerant duplex system.



(*a*) Modified switching element for the extra-stage cube network: (*b*) disabled state; (*c*) enabled state.



(*a*) 8 × 8 generalized cube network; (*b*) the corresponding extra-stage cube network.